Remarks

Reconsideration of this application is requested. By this response to the Office Action claims 1, 11-15 and 20 were amended and claims 8-10 and 23-31 were canceled. Claims 1-7 and 11-22 remain in the application.

Objection to the Abstract

The Office Action objects to the abstract of the disclosure for failing to sufficiently assist readers in deciding whether there is a need for consulting the full patent text for details. Please change the Abstract on page 12 to the following:

A nonvolatile stack is configured within a nonvolatile memory. The nonvolatile stack has a user defined stack depth configured to store instructions and/or parameter values. A memory write operation invalidates previous data stored in the nonvolatile stack.

Objection to the Disclosure

The Office Action objects to the disclosure, in particular on page 6, line 6 and line 28. Please amend the specification as shown below.

FIG. 4 describes operating features of the nonvolatile memory in accordance with the present invention. Block 410 describes data pushed onto the stack from the bottom of stack 24. For an internal block of nonvolatile memory sized to store from 0 to N data words, block 420 indicates that when the parameter value in WORD "N+2" is written, the data in WORD 0 is invalid. Block 430 shows that that the address in the offset register is incremented when stack 24 is written and that the pointer to a valid stack location is maintained. Block 440 indicates that when INTERNAL BLOCK 0 is full, data may then be written to INTERNAL BLOCK 1. Block 450 indicates that when INTERNAL BLOCK 0 is entirely invalid, INTERNAL BLOCK 0 may then be erased. Block 460 indicates that when INTERNAL BLOCK 1 is full, data may then be written to INTERNAL BLOCK 0. Block 470 indicates that when INTERNAL BLOCK 1 is entirely invalid that INTERNAL BLOCK 1 may then be erased.

The Office Action also objects to the phrase "and changes as fall" as found on page 6, line 28. This portion of Applicant's disclosure seems correct as drafted so further comments and a suggestion for a change from the Examiner would be appreciated.

Objection to the Claims

The Office Action objects to the dependent claims 12-14 and 27-31 that maintain a 'comma' after the claim number from which that claim depends. Claims 12-14 have been amended per the Examiner's suggestion and claims 27-31 have been canceled per this response.

Response to the 35 U.S.C. §101 Rejection

The Office Action rejected claims 26-31 under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. Claims 26-31 have been canceled per this response and the rejection of these claims under 35 U.S.C. §101 is now moot.

Response to the 35 U.S.C. §102(b) Rejection

The Office Action rejected claims 1-6, 11, 14-15, 17-19 and 26-31 under 35 U.S.C. §102(b) as being anticipated by Wang (U.S. Patent No. 6,449,625).

Claims 1-6

Applicant's claim 1 has been amended to recite a stack having a stack depth configured in a nonvolatile memory to store parameter values, where each memory write invalidates previous data.

Support for the amended language of claim 1 may be found in Applicant's specification on page 4, lines 22-23. In this portion of Applicant's specification Applicant states that the stack depth of stack 24 may be a parameter that is configurable through software by the system designer. Additional support for the amended language of claim 1 may be found in Applicant's specification on page 6, lines 7-12, that states subsequent data writes to stack 24 may be sequentially stored in that memory block, with each write invalidating data from a prior write. The example provided in this portion

of the specification describes a word labeled WORD Z being written to stack 24 (see FIG. 3), with the write invalidating the data in another word labeled WORD C.

The Examiner uses the prior art reference of Wang to reject Applicant's claim 1. Wang discloses in FIG. 1 a Central Processing Unit (CPU) 10 that controls a RAM 12 and a FLASH memory 14. In column 4, lines 15-17, Wang states that the FLASH memory 14 logs database transactions performed upon the database.

Wang teaches that RAM 12 maintains a copy of the database and that CPU 10 searches the physical location of the applicable records in RAM 12 to write a copy of the transaction just performed on the database to the next available memory space in FLASH memory 14. Wang in column 4, lines 39-45, teaches that a write cycle starts with the numerically addressable first block and continues until the penultimate block is filled. Following the write cycle, Wang discloses in column 4, lines 46-52, that a "garbage collection cycle" is performed to review all transactions currently stored in the FLASH memory, with only the most recent actions performed on any particular record maintained or preserved.

Thus, Wang teaches a two step process that includes a write cycle followed by a garbage collection cycle. Again, the write cycle copies transactions just performed on the database that are currently stored in the RAM to the next memory space that is available in FLASH memory 14; and the garbage collection cycle keeps the transactions stored in the FLASH memory current.

Applicant's amended claim 1 includes at least two features not taught or suggested by the prior art reference. Applicant's amended claim 1 recites a stack to store parameter values, where each memory write invalidates previous data.

A first feature not taught by Wang that is included in Applicant's claim 1 is the feature that the stack stores parameter values. Wang clearly teaches in column 4, lines 26-32, that the FLASH memory 14 only stores transactions, and names three database operations for the transactions that may be stored.

Namely, these operations represent an insert operation, an update operation and a delete operation.

A second feature not taught by Wang that is included in Applicant's claim 1 is the feature that each memory write invalidates previous data. Wang teaches a write cycle to perform numerous data transfers of Ram data to the FLASH memory, followed by a garbage collection cycle to clean up the FLASH. Wang's two staged algorithm of a write cycle and a garbage collection cycle does not teach Applicant's claimed limitation that each memory write invalidates previous data. Therefore, the prior art reference of Wang does not anticipate these two features recited in Applicant's claim 1. Accordingly, the rejection of Applicant's amended claim 1 under 35 U.S.C. §102(b) as being anticipated by Wang should be withdrawn.

Applicant's claims 2-6 depend, either directly or indirectly, from base claim 1 and are believed allowable over the prior art for at least the same reasons as Applicant's claim 1.

Claims 11 and 14

Applicant's claim 11 has been amended to overcome the rejection under 35 U.S.C. §102(b). Applicant's amended claim 11 recites a nonvolatile stack to store parameter values in words of a nonvolatile memory where a write of the nonvolatile stack invalidates previous instructions or data stored in the nonvolatile stack.

Support for the amended language of claim 11 may be found in Applicant's specification on page 3, lines 8-17. Applicant states in this portion of the specification that stack 24 retains nonvolatile stack parameter values in a nonvolatile memory that may be instructions and/or data. Further support for the amended language of claim 1 may be found in Applicant's specification on page 4, lines 11-13, that states the stack structure within the nonvolatile memory may be used to provide storage for frequency and time slot information. Thus, Applicant's specification clearly teaches that stack 24 as illustrated in FIG. 3 may store both data and instructions.

Again, Wang teaches in column 4, lines 26-32, that the FLASH memory 14 only stores transactions, and lists three database operations for the

transactions as an insert operation, an update operation and a delete operation. In contrast to Wang's teaching that the FLASH memory only stores transactions, Applicant's claim 11 recites a write of the nonvolatile stack invalidates previous instructions or data stored in the nonvolatile stack. Wang does not teach that both data and instruction may be stored in the FLASH memory. Accordingly, Wang does not anticipate Applicant's amended claim 1 and the rejection of this claim under 35 U.S.C. §102(b) as being anticipated by Wang should be withdrawn.

Applicant's claim 14 directly depends from base claim 11 and is believed allowable over the prior art for at least the same reasons as Applicant's claim 11.

Claims 15, 17-19

Applicant's claim 15 has also been amended to overcome the rejection under 35 U.S.C. §102(b). Applicant's amended claim 15 recites a storage device, comprising a nonvolatile memory having multiple blocks in a dynamic block swapped architecture, wherein a pair of blocks are configured to provide a first stack that stores data and instructions.

The amended claim language of Applicant's claim 15 for a stack that stores data and instructions finds support in the specification on page 4, lines 11-13. Applicant provides a statement that the stack structure in the nonvolatile memory may be used to provide storage for frequency and time slot information clearly shows the storage of data values. Then, Applicant's specification on page 3, lines 8-17, clearly teaches that stack 24 as illustrated in FIG. 3 may store both data and instructions.

Again, Wang only illustrates and discloses a stack structure that logs and stores transactions in the form of insert, update and delete operations. Thus, with his configuration for the stack Wang cannot anticipate Applicant's claimed feature of a nonvolatile memory having multiple blocks in a dynamic block swapped architecture, wherein a pair of blocks are configured to provide a first stack that stores data and instructions. The prior art reference of Wang is not sufficient to anticipate Applicant's claimed features recited in claim 15.

Claims 17-19 directly depend from base claim 15 and are believed allowable over the art of record for the same reasons as base claim 15.

Claims 26-31

Applicant's claims 26-31 have been canceled per this response and the rejection of these claims is now moot.

Response to the 35 U.S.C. §103(a) Rejection

Claims 7, 12-13 and 16

The Office Action rejected claims 7, 12-13 and 16 under 35 U.S.C. §103(a) as being unpatentable over Wang in view of Jou et al. (U.S. Patent No. 5,568,423).

Applicant's claim 7 depends from base claim 1 and is believed patentable over Wang in view of Jou et al. for at least the same reasons as claim 1. Claims 12-13 are dependent claims that depend from base claim 11 and are believed allowable for the same reasons as base claim 11. Claim 16 is a dependent claim from base claim 15 and is believed allowable for the same reasons as base claim 15.

Claim 8

The Office Action rejected claim 8 under 35 U.S.C. §103(a) as being unpatentable over Wang in view of Royer Jr. et al. (U.S. 2003/0061436).

Applicant's claim 8 depends from base claim 1 and is believed patentable over Wang in view of Jou et al. for at least the same reasons as claim 1.

Claims 9-10

The Office Action rejects Applicant's claims 9-10 under 35 U.S.C. §103(a) as being unpatentable over Wang in view of Lucker et al. (U.S. 2005/0114588).

Applicant's claims 9-10 have been canceled per this response and the rejection of these claims under 35 U.S.C. §103(a) is now moot.

Claims 20-22

The Office Action rejects Applicant's claims 20-22 under 35 U.S.C. §103(a) as being unpatentable over Wang in view of Lipsanen et al. (U.S. 2004/0242203).

Applicant's claim 20 has been amended per this response to overcome the teachings included in the cited prior art of record. Applicant's claim 20 recites, among other things, a nonvolatile memory coupled to the processor to provide a nonvolatile stack to store parameter values that include both data and instructions.

As previously mentioned, Wang only teaches that transactions such as an insert operation, an update operation and a delete operation are stored in his FLASH memory. The Wang reference and the Lipsanen et al. reference, either taken singularly or in combination, do not teach at least this feature of Applicant's claim 20 and the rejection under 35 U.S.C. §103(a) should be removed.

Applicant's claims 21-22 depend from claim 20 and are believed allowable for at least the same reasons as Applicant's base claim 20.

Claim 23

The Office Action rejects Applicant's claim 23 under 35 U.S.C. §103(a) as being unpatentable over Wang in view of Lipsanen et al. (U.S. 2004/0242203) and further in view of Royer Jr. et al. (U.S. 2003/0061436).

Applicant's claim 23 has been canceled per this response and the rejection of this claim under 35 U.S.C. §103(a) is now moot.

Claim 24

The Office Action rejects Applicant's claim 24 under 35 U.S.C. §103(a) as being unpatentable over Wang in view of Lipsanen et al. (U.S. 2004/0242203) and further in view of Ovshinsky et al. (U.S. Patent # 5,296,716).

Applicant's claim 24 has been canceled per this response and the rejection of this claim under 35 U.S.C. §103(a) is now moot.